WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first wiring layer having a first lower end and a first upper end protruded more than the first lower end; and

a second wiring layer having a second lower end and a second upper end protruded more than the second lower end, the second upper end facing the first upper end with the interposition of a first gap, and the second lower end facing the first lower end with the interposition of a second gap larger than the first gap.

2. The semiconductor device according to claim 1, wherein the first and second upper ends have squarish shapes.

3. The semiconductor device according to claim 1, wherein the first and second wiring layers are gate electrodes.

4. The semiconductor device according to claim 1, wherein the first and second wiring layers are gate electrodes of driver transistors facing each other in adjacent cells of an SRAM of a point-symmetrical type.

5. The semiconductor device according to claim 1, further comprising:

a semiconductor substrate which is formed below the first and second wiring layers across the first and second wiring layers; and

a silicide film which is formed on an upper surface of the semiconductor substrate between the first and second wiring layers, an upper surface of the first wiring layer, and a side face of the first wring layer opposite to the second wiring layer to electrically connect the first wiring layer to the semiconductor substrate.

6. The semiconductor device according to claim 5, further comprising a side wall insulating film which is continuously formed along side faces of the first and second wiring layers across the first and second wiring layers.

7. The semiconductor device according to claim 5, wherein the first and second wiring layers are a gate electrode of a load transistor and a gate electrode of a transfer transistor in an SRAM of a point-symmetrical type.

8. A method for manufacturing a semiconductor device, comprising:

forming a first insulating film;

selectively removing the first insulating film by anisotropic etching to form a first dummy block formed of the first insulating film in a predetermined region;

slimming the first dummy block by isotropic etching;

forming a conductive film to cover the first dummy block;

removing the conductive film until an upper surface of the first dummy block is exposed; and

patterning the conductive film to form first and second wiring layers formed of the conductive films divided by the first dummy block.

9. The method according to claim 8,

wherein the first wiring layer has a first lower end and a first upper end protruded more than the first lower end,

the second wiring layer has a second lower end and a second upper end protruded more than the second lower end,

the second upper end faces the first upper end with the interposition of a first gap, and the second lower end faces the first lower end with the interposition of a second gap larger than the first gap.

10. The method according to claim 9, wherein the first and second upper ends have squarish shapes.

11. The method according to claim 8, wherein the first and second wiring layers are gate electrodes.

12. The method according to claim 8, wherein the first and second wiring layers are gate electrodes of driver transistors facing each other in adjacent cells of an SRAM of a point-symmetrical type.

13. The method according to claim 8, further comprising:

forming a side wall insulating film on side faces of the first dummy block and the first and second wiring layers;

removing the first dummy block to expose an upper surface of an active region between the first and second wiring layers; and

forming a silicide film on the upper surface of the active region, upper surfaces of the first and second wiring layers, and opposite side faces of the first and second wiring layers.

14. The method according to claim 13, wherein the first wiring layer is electrically connected to the active region by the silicide film.

15. The method according to claim 13, wherein the first dummy block is removed with HF steam.

16. The method according to claim 13, the first and second wiring layers are a gate electrode of a load transistor and a gate electrode of a transfer transistor in an SRAM of a point-symmetrical type.

17. The method according to claim 8, further comprising, before the patterning of the conductive film:

forming a second insulating film on the conductive film;

patterning the second insulating film;

forming a side wall insulating film on a side face of the patterned second insulating film; and

removing the second insulating film,

wherein the conductive film is patterned by using the side wall insulating film as a mask.

18. The method according to claim 17,

wherein when the first dummy block is formed, a second dummy block formed of the first insulating film is formed below an end of the side wall insulating film, and the conductive film is divided by the second dummy block.

19. The method according to claim 17,

wherein the second insulating film is removed by isotropic etching.